PSIM

TUTORIAL

IGBT Level-2 Model

October 2017

The IGBT level-2 model takes into account the IGBT turn-on and turn-off transients. It provides a quick way of studying IGBT's transient behaviour.

This tutorial describes how to use the IGBT level-2 model.

Parameters needed by the model are:

Maximum Vce	Maximum rating of the collector-emitter voltage V_{ces}, in V
Maximum Vec	Maximum rating of the emitter-collector voltage V_{ecs}, in V. If IGBT has an anti-parallel diode, this voltage will be the diode forward conduction threshold voltage.
Gate Threshold Voltage	Gate threshold voltage V_{ge_th}, in V
Transconductance	Transconductance g_{fs} of the IGBT, in S
Fall Time	Fall time T_{fall} of the current when IGBT is turned off, in sec.
Capacitance C_{ies}	Input capacitance C_{ies}, in F
Capacitance C_{oes}	Output capacitance C_{oes}, in F
Capacitance C_{res}	Reverse transfer capacitance C_{res}, in F
R_{ce_on}	Collector-emitter on resistance R_{ce_on}, in Ohm
$V_{ce\_threshold}$	Collector-emitter threshold voltage V_{ce_th}, in V
Internal Gate Resistance	Internal gate resistance R_{gate}, in Ohm

To illustrate the process of obtaining the model parameters, this tutorial uses the IXYS IGBT IXXH110N65C4 (650V, 110A) as an example. This device does not have an anti-parallel diode.

Parameters V_{ces}, V_{ge_th}, g_{fs}, T_{fall}, C_{ies}, C_{res}, C_{oes}:

These parameters can be read directly from the manufacturer datasheet, as highlighted in the red boxes on the datasheet images below.

From the datasheet, we have:

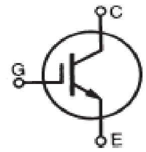
V_{ces} = 650
V_{ge_th} = 6
g_{fs} = 52
T_{fall} = 35n
C_{ies} = 5500p
C_{oes} = 267p
C_{res} = 80p

XPT™ 650V IGBT GenX4™

IXXH110N65C4

V_{CES} = 650V
I_{C110} = 110A
$V_{CE(sat)}$ ≤ 2.35V
$t_{fi(typ)}$ = 35ns

Extreme Light Punch Through IGBT for 20-60 kHz Switching



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 175°C	650	V
V_{CGR}	T_J = 25°C to 175°C, R_{GE} = 1MΩ	650	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C (Chip Capability)	235	A
I_{LRMS}	Terminal Current Limit	160	A
I_{C110}	T_C = 110°C	110	A
I_{CM}	T_C = 25°C, 1ms	600	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 150°C, R_G = 2Ω Clamped Inductive Load	I_{CM} = 220 @V_{CE} ≤ V_{CES}	A
t_{sc} (SCSOA)	V_{GE} = 15V, V_{CE} = 360V, T_J = 150°C R_G = 10Ω, Non Repetitive	10	µs
P_C	T_C = 25°C	880	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +175	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
M_d	Mounting Torque	1.13/10	Nm/lb.in.
Weight		6	g

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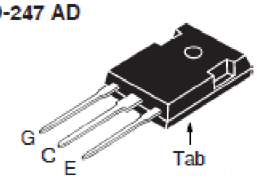


G = Gate
C = Collector
E = Emitter
Tab = Collector

Features

- Optimized for 20-60kHz Switching
- Square RBSOA
- Avalanche Capability
- Short Circuit Capability
- International Standard Package

Advantages

- High Power Density
- 175°C Rated
- Extremely Rugged
- Low Gate Drive Requirement

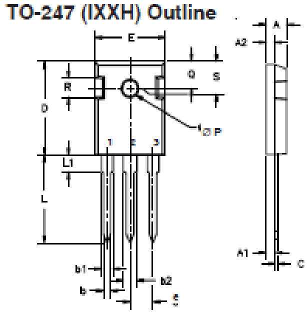
Applications

- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts
- High Frequency Power Inverters

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250µA, V_{GE} = 0V	650			V
$V_{GE(th)}$	I_C = 4mA, V_{CE} = V_{GE}	4.0		6.5	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			10	µA
	T_J = 150°C			500	µA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±100	nA
$V_{CE(sat)}$	I_C = 110A, V_{GE} = 15V, Note 1		2.06	2.35	V
	T_J = 150°C		2.50		V

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 60A, V_{CE} = 10V, Note 1	30	52		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		5500		pF
C_{oes}			267		pF
C_{res}			80		pF
$Q_{g(on)}$	I_C = 110A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		167		nC
Q_{ge}			44		nC
Q_{gc}			63		nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**		30		ns
t_{ri}	I_C = 55A, V_{GE} = 15V		45		ns
E_{on}	V_{CE} = 400V, R_G = 2Ω		2.50		mJ
$t_{d(off)}$	Note 2		110		ns
t_{fi}			35		ns
E_{off}			0.63	1.05	mJ
$t_{d(on)}$	**Inductive load, T_J = 150°C**		26		ns
t_{ri}	I_C = 55A, V_{GE} = 15V		45		ns
E_{on}	V_{CE} = 400V, R_G = 2Ω		3.55		mJ
$t_{d(off)}$	Note 2		120		ns
t_{fi}			40		ns
E_{off}			0.90		mJ
R_{thJC}				0.17	°C/W
R_{thCS}			0.21		°C/W

TO-247 (IXXH) Outline



Terminals: 1 - Gate 2 - Collector 3 - Emitter

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15 BSC		242 BSC	

Parameter V_{ecs}:

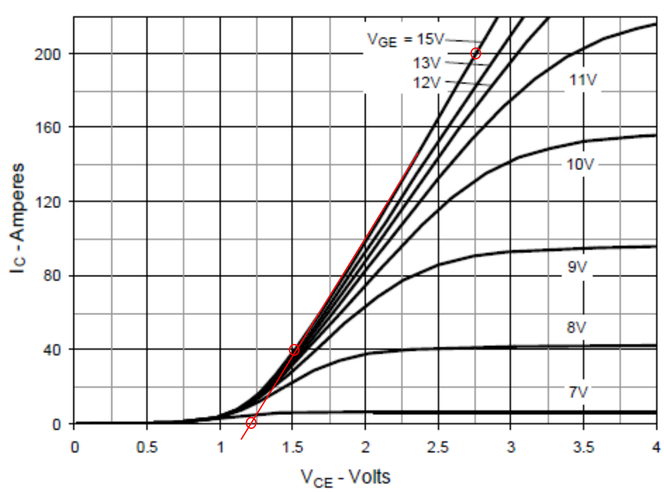
This parameter is not provided in the datasheet. We will use a typical value of 15V in this case.

If there is an anti-parallel diode, this parameter will be the diode forward conduction threshold voltage.

Parameters R_{ce_on} and V_{ce_th}:

These two parameters can be obtained from the Ic-Vce characteristics, as shown below.

Fig. 1. Output Characteristics @ T_J = 25°C



The parameter R_{ce_on} represents the slope of Vce vs. Ic, and the parameter V_{ce_th} is the voltage when Ic = 0.

We will use the curve corresponding to Vce = 15V. From the graph, we can obtain the following:

V_{ce_th} = 1.2 V

Also, based on two points from the graph, we can calculate the resistance. From the graph, we have:

V_{ce1} = 2, I_{c1} = 100; V_{ce2} = 2.75, I_{c2} = 200A

Then

R_{ce_on} = (2.75 – 2) / (200 – 100) = 7.5 mOhm

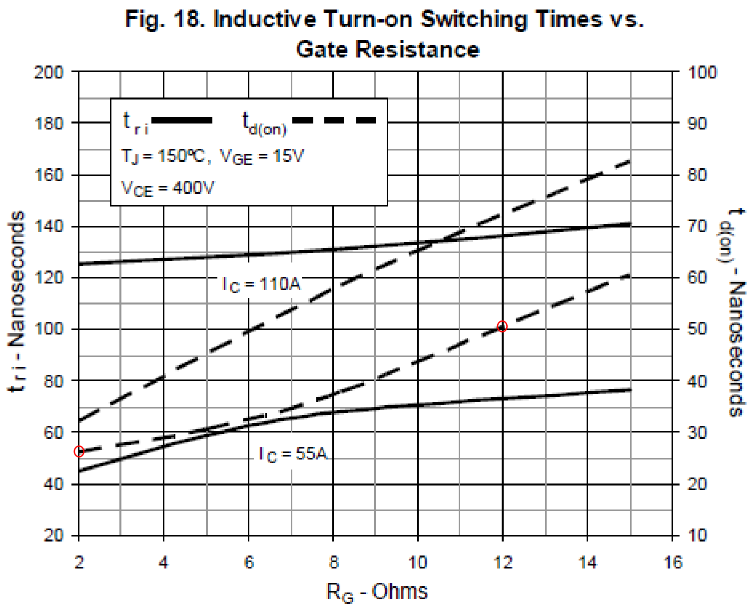
Note that the graph used here is for Tj = 25°C. To better match the circuit, the values of R_{ce_on} and V_{ce_th} may need to be adjusted for the actual operating temperature Tj.

Parameter R_{gate}:

The internal gate resistance is typically not given in a datasheet.

If the curve of the turn-on delay time t_{d_on} vs. the gate resistance R_G is given (such as in this case), the internal gate resistance can be calculated approximately from the curve. If the curve is not given, one can set up a test circuit with the same test condition as in the datasheet, and adjust the internal gate resistance until the simulation result of the turn-on time or turn-off time is close to the datasheet result.

From the datasheet, we have the switching times vs. the gate resistance as below:



The total gate resistance R_{g_total} is equal to the external gate resistance R_G plus the internal gate resistance R_{gate}. If the turn-on delay time is doubled, we can assume that the total resistance is doubled. From the graph, we have:

$t_{d\_on,1}$ = 26n, $R_{G,1}$ = 2

$t_{d\_on,2}$ = 52n, $R_{G,2}$ = 12

We have:

$R_{G,2} + R_{gate} = 2 * (R_{G,1} + R_{gate})$

Or

$R_{gate} = R_{G,2} - 2 * R_{G,1} = 12 - 2*2 = 8$

For better fit of the rise time, an internal gate resistance of 5 Ohm is used.

In general, model parameters may need to be adjusted to have a better match to the datasheet results or experimental results.