DS H01

The DS H01 is a high performance dual digital synthesizer with wide output bandwidth specially designed for Defense applications where generation of **wideband ultra-low noise signals** along with **very fast switching times** are needed.

This module has two independent outputs with more than 500 MHz bandwidth and a Spurious -Free Dynamic Range (SFDR non-harmonics) better than 70 dBc. Each output can change its frequency in less than 10 ns.

Internally, both signals can be used to feed an IQ modulator and generate a microwave signal within 1 GHz band up to the C-band.

Clocks may be internal or can be provided by the user in case of coherent signal generation with the rest of the user's system is required.

Several IOs are available (differential and single ended) to allow the user to interface the unit with the other system signals in a very straight-forward way. All IOs are electrically protected in order to support harsh environments.

The DS H01 has a very high speed Field-Programmable Gate Array (FPGA) inside to link user interface to the output signal generation allowing the customer to have a huge flexibility. A Joint Test Action Group (JTAG) connector is available to interface with the FPGA.

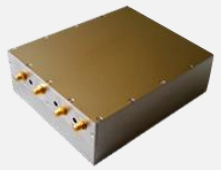
Features

- Frequency output bandwidth:
  - › Dual channel: 0.1 - 500 MHz
  - › Single channel: LO - 500 MHz to LO + 500 MHz (internal LO = 3.5 GHz)
- Phase Noise @ 320 MHz:
  - › 100 Hz offset: -115 dBc/Hz typ.
  - › Noise floor: -157 dBc/Hz typ.
- Chirp generation
- Frequency switch time: 10 ns max.
- Wideband SFDR for IQ output: 70 dBc typ. (non-harmonics)
- Frequency tuning resolution: 7.1 µHz typ.
- FSK, PSK, QAM modulations

Applications

- RADAR LO frequency generation
- Pulse compression RADAR RF pulse expander
- FMCW RADAR
- Electronic counter-countermeasures (ECCM)
- Frequency hopping
- Test & measurement

174 x 131 x 54 mm



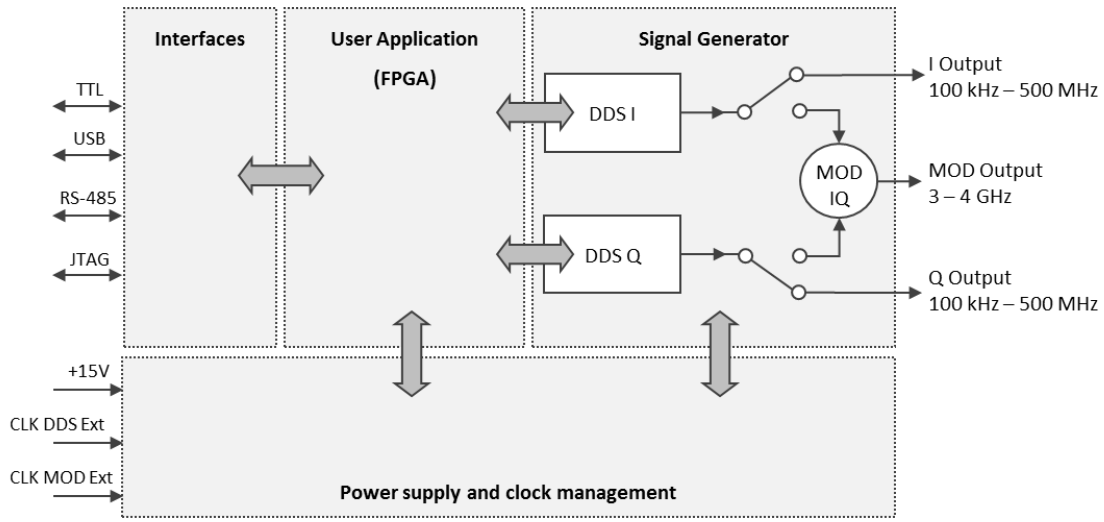
Technical Description

Functional Description

The DS H01 is composed of 4 main functional blocks :

- Interface: I/Os are protected and converted to different standards.
- Signal generator: High bandwidth signal generator with an integrated IQ modulator
- User application: User specific application linking the two others functional blocks
- Power supply and clock management: delivering clean power supplies and clocks to other functional blocks

Fig. 1: Functional Block Diagram



Interface I/O

- 12 TTL inputs or 6 RS-422 differential inputs
- 4 TTL outputs or 2 RS-422 outputs
- 1 USB interface
- 1 JTAG interface
- 1 BITE (Built-In Test Equipment) output

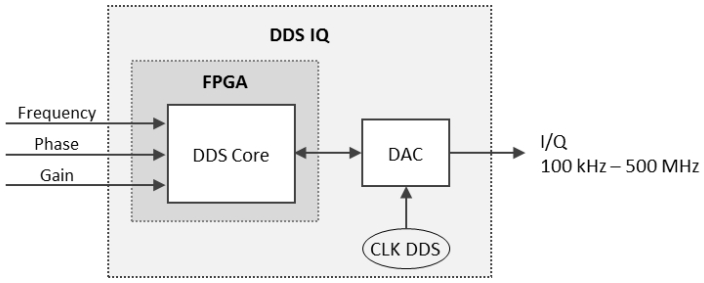
BITE signal is controlled by the user application and is OR'ed with the board power supply status. This signal can be configured as open-drain or as dry contact.

Signal Generator

The generator block uses a DDS (Direct Digital Synthesizer) scheme to synthesize the signal. A sine waveform is stored in a LUT (Look-Up Table) and then is swept to generate the output signal. The main advantage of this architecture is the speed: as the system is internally clocked at a very high frequency (CLK DDS ~2 GHz), it can change the output signal frequency in less than 10 ns. Each DDS block is composed of a DDS Core and a high speed DAC to perform the digital-to-analog conversion.

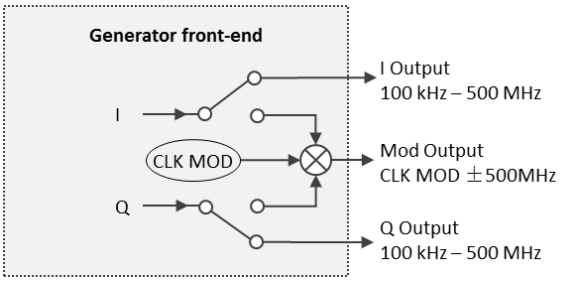
The core of the DDS is implemented inside the FPGA and interacts with the User Application using 3 data lines that allow to change frequency, phase and gain on real-time. This block also interacts with a high speed DAC which is responsible of the digital to analog conversion.

Fig. 2: DDS Core Block Diagram



Finally, the user can either route each DDS output directly to the module's output or fed them to an internal modulator for up conversion purpose. In this case, the output signal can be synthesized within a 1GHz band around the modulator center frequency (CLK MOD)

Fig. 3: IQ Modulator



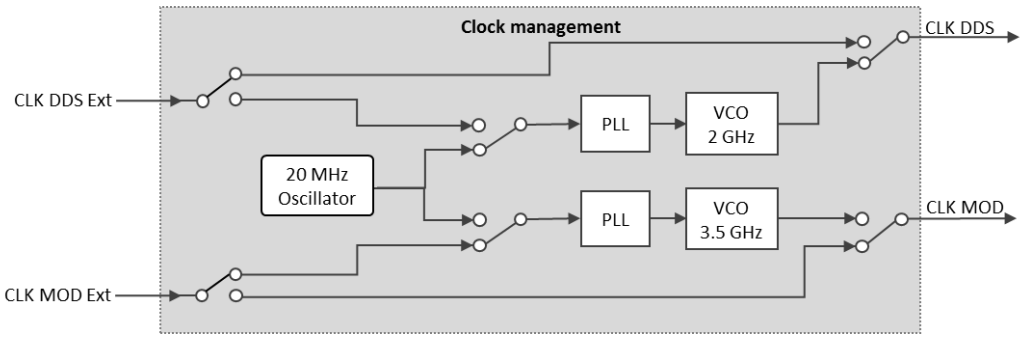
Clock management

The module proposes several clocking schemes. In order to be fully autonomous, an internal 20 MHz oscillator provides the reference to two PLLs. One drives a 2 GHz VCO for the DDS clock and the other a 3.5 GHz VCO for the IQ Modulator. However, the reference for each PLL can be provided externally in case of coherent generation required.

As the internal clocking scheme is based on VCO, the resulting phase noise on output signal is not optimized. That is why the module has the capability to shunt internal PLL and VCO, and allows the user to directly input external high frequency clocks for DDS and/or modulator. By choosing adequate low noise sources, the user can drastically improve the output phase noise. Rakon OCSOs (Oven Controlled SAW Oscillator) are best-in-class low noise solutions in the frequency range from 300 MHz up to 5 GHz, so they are perfect candidates.

All these clocking possibilities are set using the User application providing the user a very flexible way to adapt clocking to its own final application.

Fig. 4: Clocking architecture



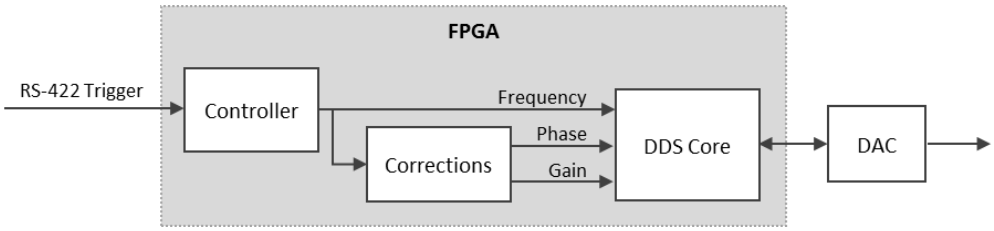
User Applications

The Frequency, Phase and Gain are available as parameters to the Customer, which opens a wide spectrum of solutions. Here are some examples of the product capabilities:

Chirp Generator

A Chirp is stored in a LUT and swept using a Controller block. This block is triggered by an external signal (normally the main ON/OFF transmission Radar's signal). A correction block is added in order to compensate Phase and Gain as frequency changes. This compensation is done real-time.

Fig. 5: Chirp Generator



FSK Modulator

Due to its very low frequency switch time, the system can be configured as FSK modulator. Digital signal to be modulated is routed using one of the differential interfaces. A controller block chooses the transmitting frequency from the value of the input.

Fig. 6: FSK Modulator

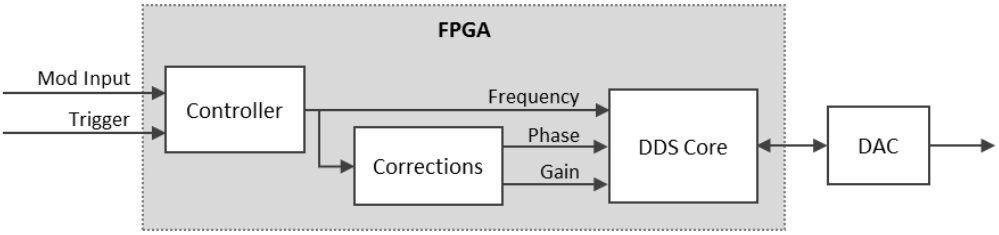
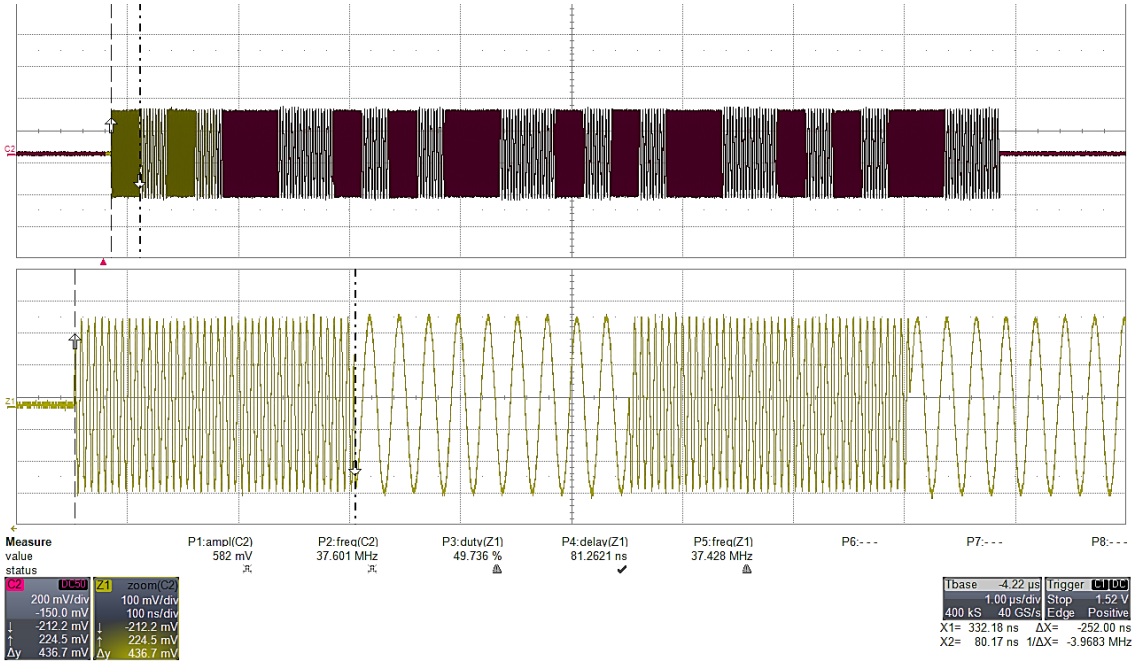


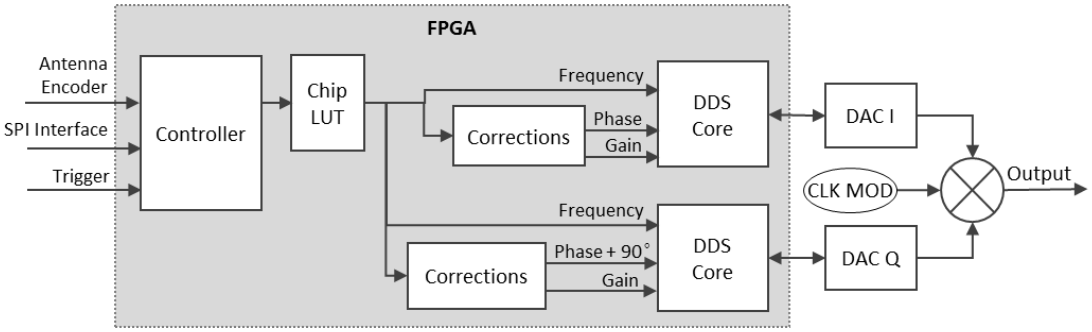
Fig. 7: The figure below shows a capture of an FSK modulated pulse of 8 µs. Bit time is approximately 250 ns



Sectored Radar Signal Generator (S-Band)

As the previous cases, a trigger signal is used to start emission. Two channels are used to upconvert the output using the modulator. The antenna encoder is fed to module in order to have a sectored configuration. An SPI interface is also provided to let the user choose the desired waveform. Output is directly upconverted to the Radar's operating frequency.

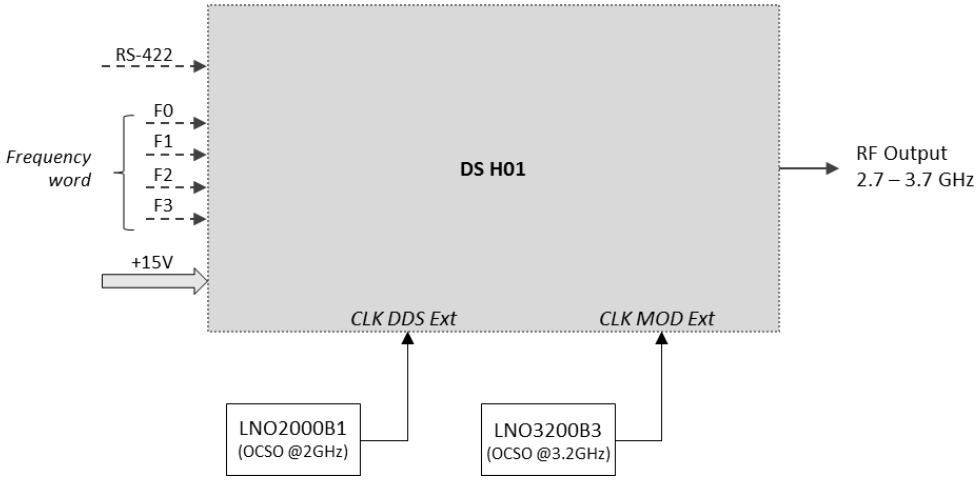
Fig. 8: Sectored Radar signal generator



High performance C-band STALO

To build a high performance C-band STALO, two ultra-low noise OSCO are used for DDS and modulator clocks. If frequency agility is required, a RS-422 link can be used to drive the frequency. Otherwise, if only discrete frequencies have to be synthesized, a hardware-coded word (up to 12 bits) is easy to implement.

Fig. 9: C-band STALO



1. Environmental Conditions[1]

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
Temperature operating		-25		+70	°C
Temperature storage		-40		+85	°C
Humidity operating	@ 30 °C, (non-condensing)			95	% RH
Shock	11 ms, 3 axes, 2 dir, half sine pulse			30	g
Random Vibration	20 to 500 Hz, 3 axes			0.1	g^2/Hz
EMI - EMC	In accordance with MIL-STD 461 F				

2. Electrical Interface

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
Supply voltage		11		16	V
Supply current	@ Power supply = 15 V		1300		mA
RF IN signal					
Type	Single				
Maximum input level				10	dBm
Impedance				1.3 : 1	VSWR
RF OUT signal					
Type	Single				
Output level			0		dBm
Impedance				1.3 : 1	VSWR
User input					
Type	RS422 / TTL				
Impedance			120		Ω
User output type	RS422 / TTL				
Bite output type	Open drain / Dry Contact				

3. Electrical Characteristics

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
IQ output BW		0.1		500	MHz
MOD output BW	With internal MOD clock	3000		4000	MHz
DDS clock input frequency		1500		2000	MHz
MOD clock input frequency		3200		3800	MHz
Frequency tuning resolution			7.1		µHz
Wideband SFDR @ IQ output			70	60	dBc
Wideband SFDR @ MOD output				40	dBc
Phase accuracy			1		mrad

[1] Procedures and conditions refer to MIL-STD-810G

4. IQ Output Performance

Fig 10: Signal Tone @ 100 MHz

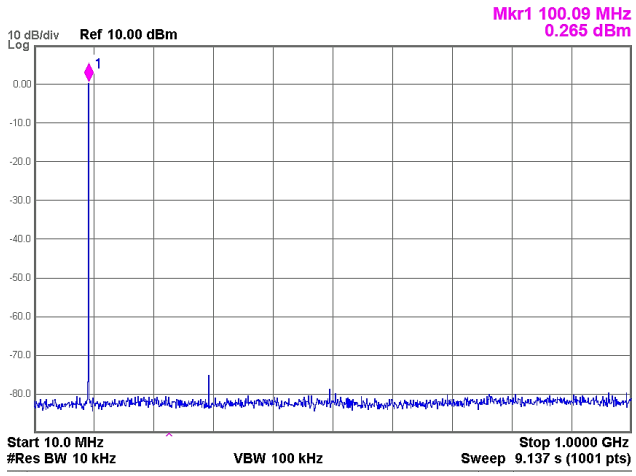


Fig 11: Signal Tone @ 200 MHz

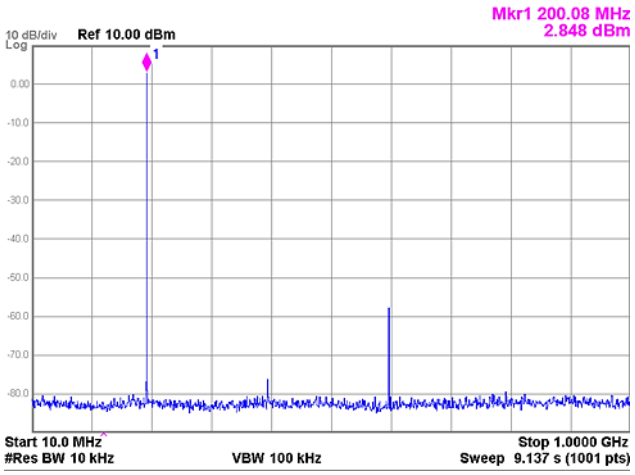


Fig 12: Signal Tone @ 300 MHz

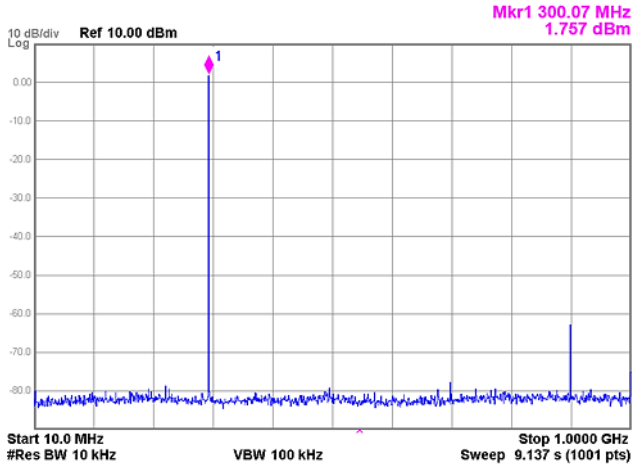


Fig 13: Signal Tone @ 400 MHz

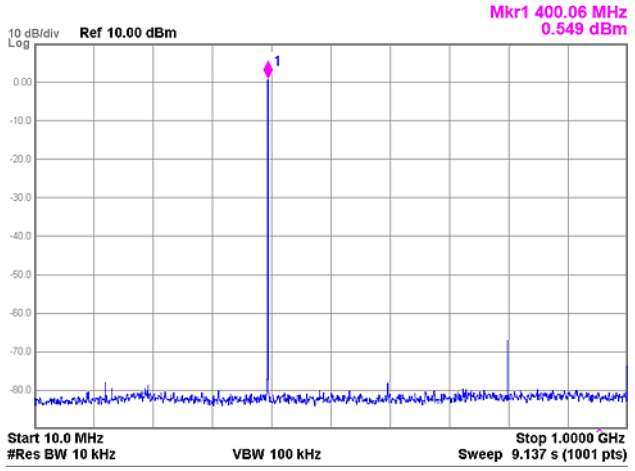
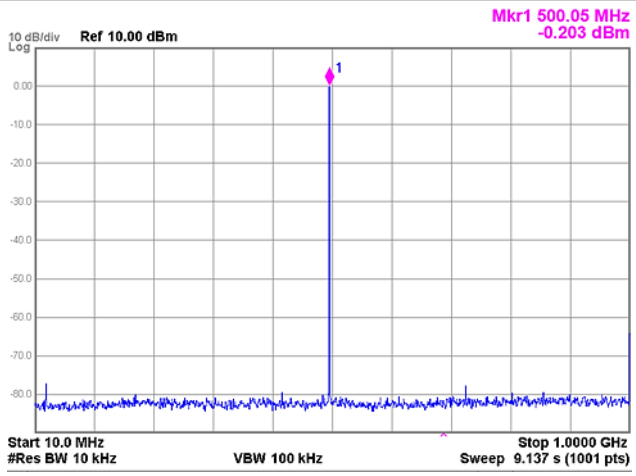


Fig 14: Signal Tone @ 500 MHz



5. Phase Noise performance

Typical value at 25°C

Parameter	320 MHz [2]	320 MHz [3]	480 MHz [2]	4000 MHz [4]	Unit
100 Hz offset	-98	-115	-96	-75	dBc/Hz
1 kHz offset	-110	-130	-104	-80	dBc/Hz
10 kHz offset	-130	-138	-126	-110	dBc/Hz
100 kHz offset	-146	-148	-142	-135	dBc/Hz
1 MHz offset	-154	-156	-152	-145	dBc/Hz

[2] Test condition: With internal DDS clock.
[3] Test condition: With external low noise (OCSO) DDS clock.
[4] Test condition: With internal DDS clock and MOD clock.

Phase noise curves

Fig 15: Phase Noise @ 320 and 480 MHz with internal DDS clock

Fig 16: Phase Noise @ 4000 MHz with internal DDS and modulator clock

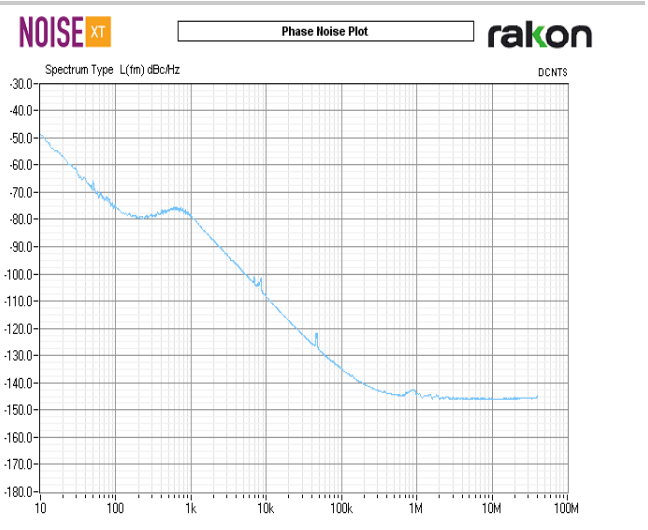
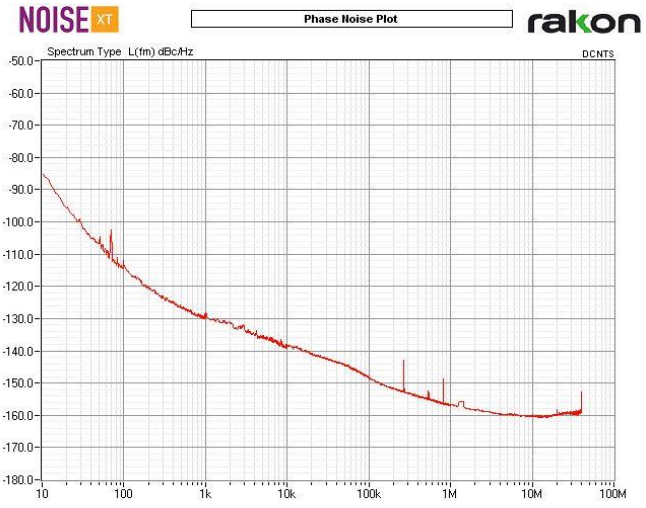


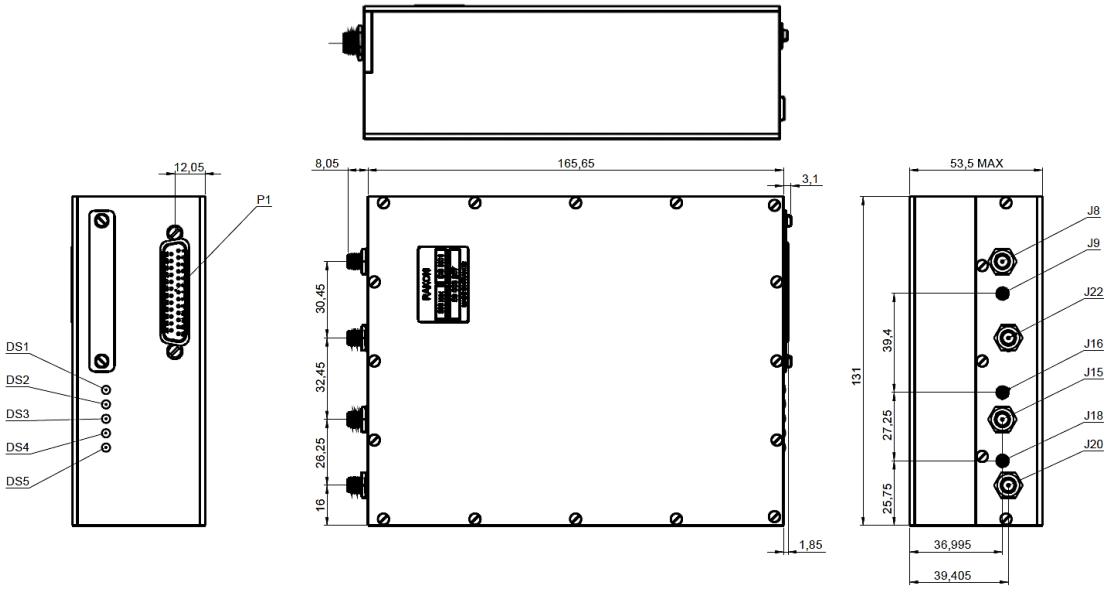
Fig 17: Phase Noise @ 320 MHz with external 2GHz DDS clock (Ultra low noise OCSO)



6. Mechanical Features and Model Outline

Parameter	Condition / Remarks	
Model outline	With connectors (typ.): 174x131x54 mm^3	Without connectors (typ.): 174x131x54 mm^3

Fig 18: DS H01 Model Outline Drawing



Unit weight	0.6 kg max.
Material	AG4.5MC
Treatment	Ni20 / Zn1
Screws	A4-70 stainless steel

7. Interfaces Description and Pin-out

Pin	Connections	Description
J8	Mod Output / I Output	Modulator Output or I Output 3 GHz ~ 4 GHz or 100 kHz ~ 500 MHz; AC, 50 Ω, SMA connector
J15	Q Output	Q Output 100 kHz ~ 500 MHz; AC, 50 Ω, SMA connector
J20	CLK DDS Ext	Clock input for DDS or reference clock 2 GHz or 20 ~ 250 MHz; AC, 50 Ω, SMA connector
J22	CLK MOD Ext	Clock input for Modulator or reference clock 3200 ~ 3800 MHz or 20 ~ 250 MHz; AC, 50 Ω, SMA connector
P1-1, 22	VCC	15 V power supply input P1: MIL-C-24308 25-pin SubD Connector
P1-14, 15	GND POW	Power supply ground
P1-3 to 5, 7 to 9, 16 to 19, 21, 22	CTRL Inputs	Input signals for control RS-422 compatible input / TTL input; 120 Ω differential impedance
P1-10, 11, 23, 24	CTRL Outputs	Output signals for control RS-422 compatible output / TTL output
P1-12, 25	BITE	BITE output Open drain or dry contact; Indicates unit OK or NOK
P1-6, 13	GND	Mechanical ground
P3	JTAG	JTAG interface for program download MOLEX type 87833-1420 connector