PLUTO+™ ULTRA STABLE SMD TCXO

RPT5032A

The RPT5032A encompasses Rakon’s new patented Pluto+ ASIC. Pluto+ advances on the world famous, Pluto ASIC technology by delivering exceptional phase noise and jitter performance, and enhanced frequency versus temperature stability. The single chip oscillator with its analogue compensation circuit is capable of sub 0.1ppm frequency stability over an extended temperature range and RMS phase jitter down to 0.13ps for IEEE1588 and SyncE applications. Its unique tilt control ensures lifetime specification compliance, unlike other TCXOs available.

Features
- Best in class frequency versus temperature
- RMS phase jitter down to 0.13ps
- Phase noise < -160dBc/Hz noise floor
- Voltage control and T-sense options available

Applications
- Time and frequency reference
  - Positioning
  - Test and Measurement
  - Telecommunications
  - Hi-Rel / Defense

5.0 x 3.2 mm

Standard Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Condition / Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal frequency</td>
<td>1.25 – 52</td>
<td>MHz</td>
<td></td>
<td></td>
<td>Standard frequencies: 10.0, 12.8, 16.384, 19.2, 19.44, 20.0, 25.0, 26.0, 30.72, 38.88 and 40MHz</td>
</tr>
<tr>
<td>Frequency calibration</td>
<td>±1</td>
<td>ppm</td>
<td></td>
<td></td>
<td>Initial accuracy at 25 ± 1°C</td>
</tr>
<tr>
<td>Reflow shift</td>
<td>±0.5</td>
<td>ppm</td>
<td></td>
<td></td>
<td>Pre to post reflow ΔF (measured ≥ 60 minutes after reflow)</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>-55 – 105</td>
<td>°C</td>
<td></td>
<td></td>
<td>Reference to (Fmax + Fmin)/2. The best available stability depends on the nominal frequency and selected operating temperature range</td>
</tr>
<tr>
<td>Frequency stability over temperature</td>
<td>±0.05 –</td>
<td>ppm</td>
<td></td>
<td></td>
<td>±5% variation Reference to frequency at nominal V&lt;sub&gt;CC&lt;/sub&gt;</td>
</tr>
<tr>
<td>Supply voltage stability</td>
<td>±0.025</td>
<td>ppm</td>
<td></td>
<td></td>
<td>±5% variation Reference to frequency at nominal V&lt;sub&gt;CC&lt;/sub&gt;</td>
</tr>
<tr>
<td>Load sensitivity</td>
<td>±0.05</td>
<td>ppm</td>
<td></td>
<td></td>
<td>• HCMOS, ACMOS: ±5pF variation, • Clipped sine wave / Sine wave: ±10% variation reference to frequency at nominal load</td>
</tr>
<tr>
<td>Long term stability (aging)</td>
<td>±1 ppm/year</td>
<td>ppm/year</td>
<td>±2 ppm/year</td>
<td></td>
<td>±3ppm/10 years ±5ppm/10 years</td>
</tr>
<tr>
<td>Acceleration Stability</td>
<td>&lt;2ppb/g</td>
<td></td>
<td></td>
<td></td>
<td>Gamma vector, 3-axes, 30-1500Hz</td>
</tr>
<tr>
<td>Start-up time</td>
<td>5 – 15 ms</td>
<td>ms</td>
<td></td>
<td></td>
<td>90% amplitude</td>
</tr>
<tr>
<td>Supply voltage, V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>2.5 V</td>
<td></td>
<td></td>
<td>V</td>
<td>±5%, standard values are 3.0, 3.3 and 5.0V</td>
</tr>
<tr>
<td>Current (C/Sine) Current (Sine)</td>
<td>2 mA</td>
<td></td>
<td>8 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current (HCMOS) Current (ACMOS)</td>
<td>4 mA</td>
<td></td>
<td>8 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Control voltage, V&lt;sub&gt;c&lt;/sub&gt;</td>
<td>0.5 V</td>
<td></td>
<td>2.5 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency tuning</td>
<td>±5 ppm</td>
<td>ppm</td>
<td>±7 ppm</td>
<td>ppm</td>
<td>tau = 1.0s</td>
</tr>
<tr>
<td>Root Allan Variance (20MHz)</td>
<td>5 10&lt;sup&gt;-11&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td>Clipped sine wave, sine wave, HCMOS (LVC莫斯 &amp; LVTTL compatible as per JESD8C) and ACMOS</td>
</tr>
<tr>
<td>Oscillator output options</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tri-State Control</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Device disabled, output in high impedance state Device enabled, operating</td>
</tr>
<tr>
<td>Input level low (pin 6)</td>
<td>0.6V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td>0.2V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input level high (pin 6)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

www.rakon.com sales@rakon.com
SSB Phase Noise (Typical value at 25°C)

![SSB Phase Noise Graphs](image)

Model Outline and Recommended Pad Layout

![Model Outline and Pad Layout](image)

**RECOMMENDED PAD LAYOUT**

- **TOP VIEW**
  - To GND
  - External Bypass Cap 100nF

- **BOTTOM VIEW**
  - 0.80 x 0.80 (x 4)
  - 0.80 x 0.70 (x 2)

**PIN CONNECTIONS**

1. * Do Not Connect / Vcc
2. GND
3. * Do Not Connect / Vref / Vtamp
4. RF Output
5. Vcc
6. Enable

* Depending on specification

- Unit: mm
- The area between the pads is a keep-out area, no tracks or ground plane allowed on any layer

Test Circuit

![Test Circuit Diagram](image)

- **Enable**
- **Vcc**
- **GND**
- **Vc for TCVCXO**
- **Do Not Connect for TCXO** (Depending on specification)

- **Probe**
- **Oscilloscope**
- **Frequency Counter**

**Reference Voltage Output**
- or **Temperature Sensor Output** (Depending on specification)

**Output Load**

- **C1**: 10pF
- **RL**: ∞

- **HCMOS & ACMS**: 10pF, 10kΩ

* Inclusive of probe impedance